CLAIMS

1. A transmitter for generating first and second modulation signals in response to first and second input data symbols in a communication system, said transmitter comprising:

a transmitter memory for storing a code sequence;

a first time shifting means for time-shifting said code sequence by a first time-shift, said first time-shift being determined by said first data symbol, said first shifting means being coupled to said transmitter memory and generating a first encoded sequence; and

a second time shifting means for reversing and time-shifting said code sequence by a second time-shift, said second time-shift being determined by said second data symbol, said second shifting means being coupled to said transmitter memory and generating a second encoded sequence.

2. A transmitter in accordance with claim 1, further comprising a quadrature modulator for generating transmitted modulated signal in response to said first and second modulation signals.

3. A transmitter in accordance with claim 1, further comprising:

a radio frequency signal generator for generating a in-phase radio frequency signal;

a phase-shifter coupled to said radio frequency signal generator for phase shifting said in-phase radio frequency signal and producing a quadrature radio frequency signal;

a first multiplier for multiplying said in-phase radio frequency signal and said first modulation signal to produce an in-phase signal component;

a second multiplier for multiplying said quadrature radio frequency signal and said second modulation signal to produce a quadrature signal component; and

a summer for summing said in-phase signal component with said quadrature signal component to produce an output signal.

4. A transmitter in accordance with claim 1 further comprising a means for converting an input bit-stream into a sequence of first and second input data symbols and said receiver further comprises a means for converting said first and second output data symbols into an output chip-stream.

5. A transmitter in accordance with claim 1, wherein said code sequence comprises M-chips, and said transmitter memory comprises an M-chip shift register for time shifting said code sequence.

6. A transmitter in accordance with claim 1, further comprising first and second pulse shapers for converting said first and second encoded sequences into said first and second modulation signals.

7. A receiver for decoding a complex modulated signal, said receiver comprising:

a receiver memory for storing a code sequence;

a first correlator coupled to said receiver memory for determining the correlation between a time-shifted version of said code sequence and said complex modulated signal; and

a second correlator coupled to said receiver memory for determining the correlation between a time-shifted and time-reversed version of said code sequence and said complex modulated signal.

8. A receiver in accordance with claim 7, said receiver further comprising:

an M-chip shift register for storing and time-shifting an M-chip code sequence;

an M-chip complex register for storing said complex modulated signal.

a first multiplier means for multiplying the code sequence stored in the M-chip shift register by the complex modulated signal stored in the M-chip complex register to generate first multiplier outputs;

a first summer for summing the first multiplier outputs to produce a first correlation signal;

a second multiplier means for multiplying the reverse of the code sequence stored in the M-chip shift register by the complex modulated

signal stored in the M-chip complex register to generate second multiplier outputs; and

a second summer for summing the second multiplier outputs to produce a second correlation signal.

9. A receiver in accordance with claim 7, further comprising:

a first peak detector for detecting a peak in said first correlation signal;

means responsive to said first peak detector and said receiver memory for recovering said first output data symbol;

a second peak detector for detecting a peak in said second correlation signal; and

means responsive to said second peak detector and said receiver memory for recovering said second output data symbol.

10. A receiver in accordance with claim 7, further comprising a quadrature down-converter for converting a received modulated signal into said complex modulated signal.

11. A communication system, comprising:

a transmitter for generating first and second modulation signals in response to first and second input data symbols, said transmitter comprising:

a transmitter memory for storing a code sequence;

a first time shifting means for time-shifting said code sequence by a first time-shift, said first time-shift being determined by said first data symbol, said first shifting means being coupled to said transmitter memory and generating a first encoded sequence; and

a second time shifting means for reversing and time-shifting said code sequence by a second time-shift, said second time-shift being determined by said second data symbol, said second shifting means being coupled to said transmitter memory and generating a second encoded sequence;

a receiver for decoding a complex modulated signal, said receiver comprising:

a receiver memory for storing a code sequence;

a first correlator coupled to said receiver memory for determining the correlation between a time-shifted version of said code sequence and said complex modulated signal; and

a second correlator coupled to said receiver memory for determining the correlation between a time-shifted and time-reversed version of said code sequence and said complex modulated signal.

12. A communication transmitter for generating first and second modulation signals in response to first and second input data symbols, said transmitter comprising:

a transmitter memory for storing a code sequence;

a time-shifting means for time-shifting said code sequence by a time-shift, said time-shift being determined by said first or second data symbol, said shifting means being coupled to said transmitter memory and generating an encoded sequence corresponding to said first or second data symbol;

a bi-directional register operable to store said encoded sequence, said bi-directional register having first and second read directions; and

a selector operable to select said first or second read directions according to whether said encoded sequence corresponds to said first or second data symbol;

wherein said first modulation signal is generated when said first read direction is selected and said second modulation signal is generated when said second read direction is selected.

13. A receiver for decoding a complex modulation signal in a communication receiver to recover a data value, said receiver comprising:

an M-chip shift register for storing and time shifting an M-chip code sequence;

a bi-directional register operable to store said complex modulation sequence, said bi-directional register having first and second write directions;

a selector coupled to said bi-directional register and operable to select between said first and second write directions;

a correlator coupled to said bi-directional register and said M-chip shift register and operable to correlate said complex modulation signal with said M-chip code sequence to produce a correlation signal;

a peak detector for detecting a peak in said correlation signal; and

means responsive to said peak detector and said M-chip shift register for recovering said data value.

14. A method for encoding first and second input data symbols, each input data symbol having one of N values, said method comprising:

storing a pseudo-noise code sequence in a memory;

time-shifting said pseudo-noise code sequence by an amount determined by the first input symbol to obtain M chips of an in-phase encoded digital signal; and

time-shifting the time-reversal of said pseudo-noise code sequence by an amount determined by the second input symbol to obtain M chips of a quadrature encoded digital signal;

15. A method in accordance with claim 14, further comprising:

converting said in-phase and quadrature encoded digital signals into in-phase and quadrature signals; and

modulating an in-phase component of a carrier signal by said in-phase signal;

modulating a quadrature component of a carrier signal by said quadrature signal; and

summing said in-phase and quadrature components of the carrier signal to produce a modulated signal.

16. A method in accordance with claim 14, further comprising converting an input bit-stream into said first and second input data symbols.

17. A method for decoding a complex code position modulated signal, said signal representing in-phase and quadrature encoded symbols, said method comprising:

storing a pseudo-noise code sequence in a memory;

generating time-shifted versions of said pseudo-noise code sequence;

determining a first correlation between the time-shifted versions of the pseudo-noise code sequence and the complex code position modulated signal;

determining the time shift that satisfies a first predetermined correlation criteria, thereby decoding said in-phase encoded symbol;

determining a second correlation between the time-shifted versions of the time reversal of the pseudo-noise code sequence and the complex code position modulated signal; and

determining the time shift that satisfies a second predetermined correlation criteria, thereby decoding said quadrature encoded symbol.

18. A method in accordance with claim 17, wherein said memory is an M-chip shift register and wherein determining a first correlation comprises:

storing said complex code position modulated signal in a second memory; and for each of N clock cycles:

performing a vector multiplication of the contents of said first memory with the contents of said second memory to obtain M first products;

adding the M first products to determine the first correlation; and

causing a circular shift of the contents of the M-chip shift register by one or more chips.

19. A method in accordance with claim 17, wherein said memory is an M-chip shift register and wherein determining a second correlation comprises:

storing said complex code position modulated signal in a second memory; and for each of N clock cycles:

performing a vector multiplication of the contents of said first memory with the time-reversal of the contents of said second memory to obtain M second products;

adding the M second products to determine the second correlation; and

causing a circular shift of the contents of the M-chip shift register by one or more chips.

20. A method in accordance with claim 17, wherein said complex code position modulated signal is generated by:

receiving a modulated signal; and

down-converting said modulated signal in a quadrature down-converter to obtain an in-phase component and a quadrature component, said an in-phase component and a quadrature components representing the real and imaginary parts, respectively, of said complex code position modulated signal.

21. A method in accordance with claim 20, further comprising passing said complex code position modulated signal through a matched filter.